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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/616,881	07/10/2003	Anthony Gus Aipperspach	AUS920020713US1	2638
7590 06/28/2005			EXAMINER	
Gregory W. Ca	rr		DO, TH	UAN V
670 Founders Sq			ART UNIT	PAPER NUMBER
900 Jackson Street Dallas, TX 75202			2825	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

	Application No.	Applicant(s)				
Office Action Summan	10/616,881	AIPPERSPACH ET AL.				
Office Action Summary	Examiner	Art Unit				
	Thuan Do	2825				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	6(a). In no event, however, may a reply be tim within the statutory minimum of thirty (30) days ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONED	ely filed s will be considered timely. the mailing date of this communication. O (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 13 June 2005.						
2a) ☐ This action is FINAL . 2b) ☐ This	This action is FINAL. 2b)⊠ This action is non-final.					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-21</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-21</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>10 July 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the c	* * * * * * * * * * * * * * * * * * * *					
Replacement drawing sheet(s) including the correcting 11) The oath or declaration is objected to by the Experience.		• • • • • • • • • • • • • • • • • • • •				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s)	•					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa					
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Application/Control Number: 10/616,881 Page 2

Art Unit: 2825

DETAILED ACTION

1. This non-final office action is responsive to amendment of restriction entered on 06/13/05. Claims 1-21 are pending in this office action.

Claim objections

Claim 1, the terms "larger than a maximum clock pulse width" and "limiting the clock pulse width"; and

Claim 3, term "relaying the clock pulse to the circuit without changing the clock pulse width"; and

Claim 4, term "preventing the circuit from being exposed to testing environments"; and

Claim 19, the term "an override signal coupled to the switch for by passing the pulse-limiting circuit".

are unclear to what applicants intend to mean within specification.

Clarification or correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

- (e) the invention was described in-
- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Application/Control Number: 10/616,881 Page 3

Art Unit: 2825

2. Claims 1-3,5-9,11-15,17,18 are rejected under 35 U.S.C. 102(e) as being unpatentable over Horan et al. Pat. No. 6704908.

Regarding claim 1: Horan teaches a method for circuit design (col. 1, lines 10-12) comprising:

detecting the clock pulse width of the clock signal (col. 7, lines 61-67 using a selection of output clocks with a minimum pulse width);

determining whether the clock pulse width is larger than a maximum clock pulse width (col. 7, lines 26-67 by determining the proper VCO output and using pulse widths and/or phase adjustments); and

upon a determination that the clock pulse width is larger than a maximum clock pulse width, limiting the clock pulse width of the clock signal (col. 7, lines 26-67).

Regarding claim 7: Horan teaches an apparatus comprising:

means for detecting the clock pulse width of the clock signal (col. 7, lines 26-67); means for determining whether the clock pulse width is larger than a maximum clock pulse width (col. 7, lines 26-67); and

means for, upon a determination that the clock pulse width is larger than a minimum clock pulse width, limiting the clock pulse width of the clock signal (col. 7, lines 26-67).

Regarding claim 13: Horan teaches a program (col. 7, lines 26-32 by executing a software) comprising:

computer program code for detecting the clock pulse width of the clock signal (col. 7, lines 26-67);

computer program code for determining whether the clock pulse width is larger than a maximum clock pulse width (col. 7, lines 26-67); and

computer program code for, upon a determination that the clock pulse width is larger than a maximum clock pulse width, limiting the clock pulse width of the clock signal (col. 7, lines 26-67).

Art Unit: 2825

The remaining claims of 102(e) section contain features similar to the rejection of claims 1,7 or 13 and rejected in the rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103 that form the basis for the rejections under this section made in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 4,10,16,19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al. Pat. No. 6704908 in view of Hogan et al. Pat. No. 5535337.

Regarding claims 4, 10, 16: However, Horan does not teach testing. Hogan teaches this feature at column 3, lines 50-51.

It would have been obvious to one of ordinary skill in the integrated circuit design art at the time of the invention to have combined the teaching of Hogan into Horan to have testing function as taught by Hogan would have provided a stable condition of circuit function.

Regarding claims 19-21: Horan teaches an apparatus of claim 7 comprising: a phase locked loop (PLL) for generating the clock signal (col. 1, lines 10-12); a pulse-limiting circuit coupled to the PLL (col. 7, lines 26-67);

a switch coupled to both the PLL and the pulse-limiting circuit (col. 7, lines 26-67 and fig. 5); and

However, Horan does not teach an override signal coupled to the switch. Hogan teaches this feature Figure 4, at least boxes 56,59,61.

It would have been obvious to one of ordinary skill in the integrated circuit design art at the time of the invention to have combined the teaching of Hogan into Horan to

Art Unit: 2825

have an override signal coupled to the switch as taught by Hogan would have provided a selection mode for an override signal.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Do whose telephone number is 571-272-1891. The examiner can normally be reached on Monday-Friday 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are 703 305-3431 for regular communications and 703-305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0596.

Thuan Do Primary examiner

Mundo

06/22/2005